Due to high electron mobility and small leakage current, InGaAs nanowires (NWs) have recently attracted tremendous interests as promising channel materials for high-performance nanoelectronics. For example, vertical wrapgate transistors with InGaAs NW arrays as the core channel materials have been demonstrated on Si with extraordinary electrical characteristics. In future, the aggressive diameter scaling of NWs will be adopted to further improve the gate electrostatic control as well as lower the off-state current; however, this scaling will also inevitably introduce more surface scattering and higher surface carrier recombination, which are detrimental to the transistor behavior. In this regard, the dependence of carrier mobility on NW diameters suggests an important design consideration of nanowire dimension to achieve the optimal device performances. To date, experimental studies on the diameter-dependent electron mobility of Si and InAs NWs have illustrated that the mobility was reduced significantly for smaller NW diameters while such diameter scaling. All these results reveal the impact of surface roughness scattering on the electron mobility. This work highlights the impact of surface roughness scattering on the electron mobility. This work suggests a careful design consideration of nanowire dimension is required for achieving the optimal device performances. © 2013 American Institute of Physics. [http://dx.doi.org/10.1063/1.4794414]
NWs characterized, which highly indicates the well-controlled NW surface morphology achieved in our simple growth method as well as the consistent surface roughness of NWs in this comparison study. More importantly, all these findings can lead us to the accurate determination of NW diameters for the mobility calculation.

After characterizing the diameter and morphology, the NW field-effect transistors (FETs) are then fabricated with standard lithography on drop-casted substrates, followed by the Ni source/drain (S/D) electrode (50 nm thick) deposition and lift-off process. The schematic of such back-gated FET structure is shown in the inset of Figure 3(a), while the main panel contains the transfer characteristics of FETs made of NWs with three different diameters, \( d = 19.3, 32.4, \) and 41.9 nm, after oxide deduction. Notably, the long channel lengths (>1 \( \mu \)m) are used to ensure the diffusive transport of carriers (rather than ballistic or quasi-ballistic transport) assessed in this work, from which intrinsic transport properties, such as carrier mobility, can be deduced. In any case, the normalized current is observed to be higher for the thicker NWs, which could be attributed to the increased effective channel width and more electron transport modes (i.e., sub-bands) get involved, but the effect of less surface and phonon scattering of larger NWs should not be neglected as well.12

Furthermore, as depicted in Figures 3(b)–3(d), all devices exhibit the linear \( I_{DS}-V_{DS} \) behavior under \( V_{DS} = 0.1 \) V, which confirms the ohmic contact formation with Ni S/D electrodes for each NW dimension. Combining with the minimized electrical hysteresis observed in this ambient measuring environment (Figure 3(a)), all these can provide a more accurate assessment of the transconductance here.14–17

Next, to assess the electron field-effect mobility (\( \mu \)) of InAs NWs, we utilize the standard square law model, \( \mu = g_m(L^2/C_{ox})(1/V_{DS}) \), where transconductance \( g_m = (dI_{DS})/(dV_{GS}) \) at a constant \( V_{DS} \) and \( C_{ox} \) is the gate capacitance, which is calculated from finite element analysis software
COMSOL. As shown in Figure 3(e), the peak mobility is estimated \(-4500, 3000, \text{ and } 1400 \text{ cm}^2 \text{ V}^{-1} \text{s}^{-1}\) for these representative thick, medium, and thin NWs, respectively. Besides this clear difference in the mobility, the peak positions of these curves are also distinctive as they are located at \(-0, 3, \text{ and } 5 \text{ V}\) for NWs with \(d = 41.9, 32.4, \text{ and } 19.3 \text{ nm}\), accordingly. This size-dependent phenomenon could be attributed to the higher gate field that leads to an enhanced surface scattering in smaller diameter of NWs.\(^{18,19}\) More importantly, as demonstrated in Figure 3(f), the statistically summarized peak field-effect mobility of 93 \(\text{In}_{0.7}\text{Ga}_{0.3}\text{As}\) NWFETs as a function of NW diameter (\(d\) spanning from 14 to 54 nm) clearly shows a monotonic increase of mobility as NW dimension becomes larger. This is possibly due to the enhanced surface scattering in smaller NWs but also the phonon scattering and thermally activated surface/interface traps. Notably, the slope of this function (mobility versus NW diameter) is found to be \(-133 (\text{cm}^2 \text{V}^{-1} \text{s}^{-1})/\text{nm}\), which is significantly lower than the reported value of state-of-the-art InAs NWs,\(^{12}\) suggesting a less sensitive geometrical degradation of mobility for the design consideration of scaled NW transistors.

In order to shed light on the nature of this mobility reduction in smaller NWs, we employ low temperature I-V measurement to further study the diameter dependent behaviors. Figure 4(a) shows the temperature dependent transfer characteristics of a NWFET with a diameter, \(d = 40.0 \text{ nm}\) and channel length, \(L = 9.9 \mu\text{m}\). It is worth noting that the threshold voltages shift towards the more positive end when temperature lowers, which could be assigned to the less activated surface/interface traps under low temperatures. Moreover, the average mobility of NWs with similar dimension (\(d \approx 40 \text{ nm}\)) exhibit a first-rapid increase (from \(-4000 \text{ to } \sim 6000 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}\)) and then towards saturation behavior (\(-7500 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}\)) as the temperature lowers from 298 to 77 K as shown in Figure 4(b). This significant mobility enhancement is diminished below 150 K, suggesting that the phonon and surface/interface traps are already frozen out at such low temperature. At the same time, the dependency of mobility on the NW dimension is also investigated at different temperatures, and the data for 11 NWFETs with \(d = 20 \text{ to } 40 \text{ nm}\) at both 298 and 77 K are presented in Figure 4(c). Specifically, at 77 K where the phonon and traps were illustrated to play insignificant effect in the mobility reduction, there is still a clear monotonic increase of mobility with the NW diameters. Also, impurity scattering should not be a factor here since the NWs are not grown with any intentional doping. As a result, this observed dependency of electron mobility on NW dimension is mainly attributed to...
In conclusion, a systematic study of the diameter-dependent electron mobility in InGaAs NWs is presented. The NWs are shown to have good crystallinity and In-rich stoichiometry while the AFM characterization provides a precise estimation of the NW diameter. By exploring the electrical characteristics of the back-gated NWFETs, the peak electron field-effect mobility is found to decrease as the NW diameter reduces. Also, low temperature measurements are performed in order to decouple the effects of surface/interface traps as well as phonon scattering and again confirm that the enhanced surface roughness scattering induces the mobility degradation in miniaturized NWs. This work suggests a careful device design consideration of nanowire dimension is required for achieving the optimal NW device performances.

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